Explanations

1. It is because in forward biased condition, the potential barrier is low in a p-n junction as compared to that in reverse biased condition. So, the resistance is low in forward biasing as compared to that in reverse biasing.

2. No, two different slabs of p-type and n-type semiconductor cannot be physically joined to form p-n junction. It is because, two different slabs have different extent of doping of impurity atom in them. So, the characteristics of a p-n junction diode are not met by this process.

3. Rectify

4. Conductivity **(1)**

5. Resistance of a material can be found out by the slope of the curve *V versus I*. Part *BC* of the curve shows the negative resistance as in this region current decreases by increasing the voltage. **(1)**

6.

n-type Semiconductor	p-type Semiconductor
It is formed by doping pentavalent impurities with tetravalent atoms.	It is formed by doping trivalent impurities with tetravalent atoms. **(1/2)**
The electrons are majority carriers and holes are minority carriers. $(n_e >> n_h)$	The holes are majority carriers and electrons are minority carriers $(n_h >> n_e)$ **(1/2)**

7. (i) Width of depletion layer decreases in forward bias. **(1/2)**

(ii) Width of depletion layer increases in reverse bias. **(1/2)**

8. In this way, continuous contact cannot be produced at atomic level and junction will behave as a discontinuity for the flowing charge carrier. **(1)**

9. When some desirable impurity is added to intrinsic semiconductor deliberately to increase its conductivity, then this process is called doping and the impurity are called dopants.

Two types of dopants (atoms) are used in doping

(i) Trivalent atoms having 3 valance electrons e.g., Indium, Boron, Aluminium, etc.

(ii) Pentavalent atoms having 5 valance electrons e.g., Arsenic, Antimony, phosphorous, etc.

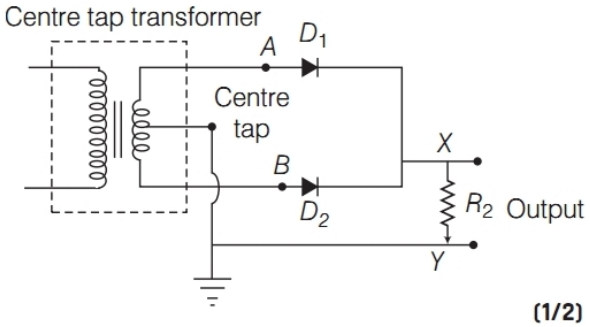
10. Refer to text on page 404 (Formation of depletion region in p-n junction) .

11. Refer to text on page 404 (Formation of depletion region in p-n junction).

12. (i) Since, isolated atoms have discrete energy levels. In a crystalline solid, due to the presence of a large number of atoms, interatomic interactions take place. Due to this, energy levels get modified to energy bands.

(ii) Refer to text on page 402.

13. A rectifier is used to convert alternating current into direct current, whose labelled circuit is given below.

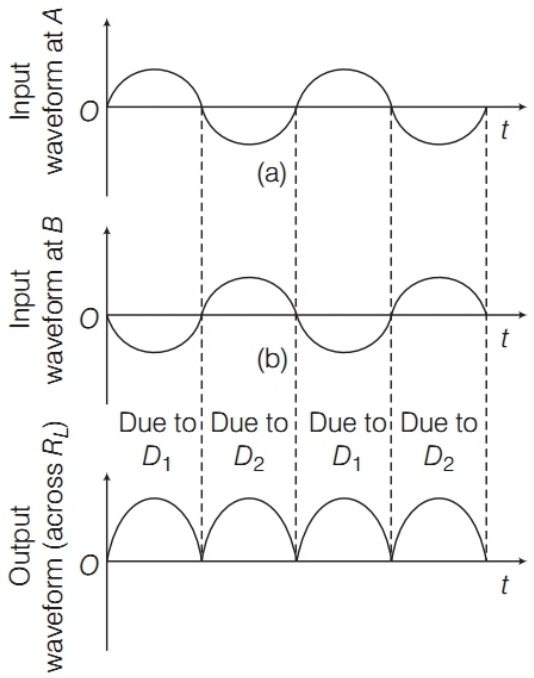


(1/2)

Working

During the positive half cycle of the input AC, the diode D_1 is forward biased and the diode D_2 is reverse biased. The forward current flows through diode D_1.

During the negative half cycle of the input AC, the diode D_1 is reverse biased and diode D_2 is forward biased. Thus, current flows through diode D_2. Thus, we find that during both the halves, current flows in the same direction. **(1)**



(1/2)

14. (i) From the given curve, we have

Voltage, $V = 0.7$ V for current,

$I = 15\,\text{mA}$ for voltage,

$\therefore$ Resistance, $\frac{V}{I} = \frac{0.7}{15\times10^{-3}} = 47\Omega$ **(1)**

(ii) For $V = -10$ V, we have

$I = -1\,\mu\text{A} = -1\times10^{-6}\text{A}$

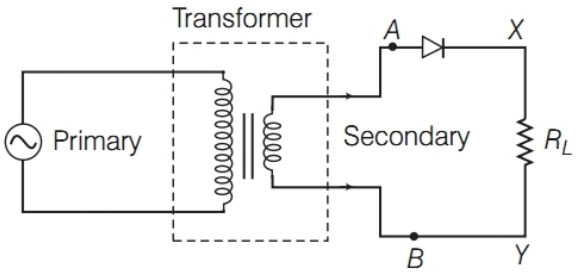
$\Rightarrow \quad R = \frac{10}{1\times10^{-6}} = 1.0\times10^{7}\Omega$ **(1)**

15.

Intrinsic semiconductor	Extrinsic semiconductor
It is a pure semiconductor material with no impurity atoms in it.	It is prepared by doping a small quantity of impurity atoms to the pure semiconductor.
The number of free electrons in the conduction band and the number of holes in valence band is exactly equal. $n_e = n_h = n_i$	The number of free electrons and holes is never equal. There is an excess of electrons $n_e > n_i$ in n-type semiconductors and excess of holes $n_h > n_i$ in p-type semiconductors.

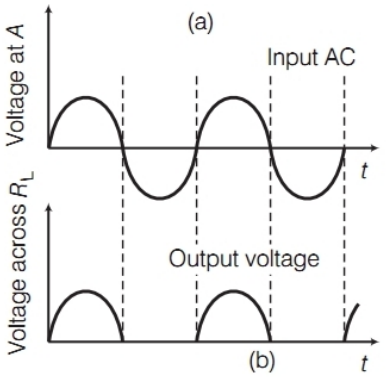
16. ***p-n* Junction Diode as a Half-Wave Rectifier**

AC voltage to be rectified is connected to the primary coil of a step-down transformer. Secondary coil is connected to the diode through resistors R_L, across which output is obtained.



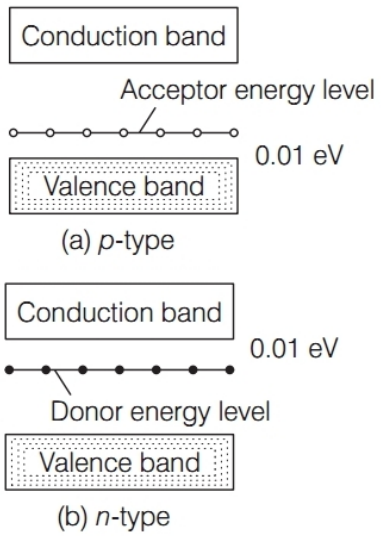
(1)

Working During positive half cycle of the input AC, the p-n junction is forward biased. Thus, the resistance in p-n junction becomes low and current flows. Hence, we get output in the load. During negative half cycle of the input AC, the p-n junction is reverse biased. Thus, the resistance of p-n junction is high and current does not flow. Hence, no output in the load. So, for complete cycle of AC, current flows through the load resistance in the same direction.



(1)

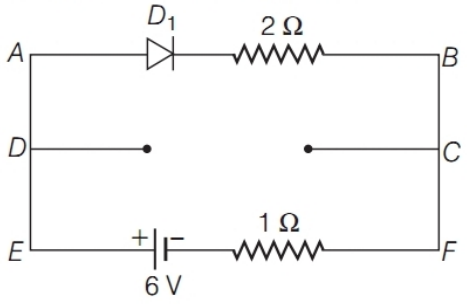
17. The required energy band diagram is shown below **(1)**



(2)

18. Refer to text on page 402 (Difference between conductor, insulator and semiconductor on the basis of energy bands).

19. According to given circuit diagram, diode D_2 is in reverse biased, hence is ineffective. Therefore redrawing the circuit diagram as



Resistances 2 Ω and 1 Ω are in series,

$$R = 2+1 = 3\ \Omega$$

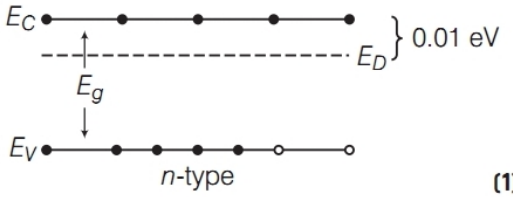
∴ Current through 1 Ω resistance,

$$I = \frac{V}{R} = \frac{6}{3} = 2\,\text{A}$$ **(2)**

20. Characteristics features of *n*-type semiconductor

(i) In *n*-type semiconductor, the semiconductor is doped with pentavalent impurity in it. The electrons are majority carriers and holes are minority carriers or $n_e >> n_h$ (n_e = number density of electrons, n_h = number density of holes).

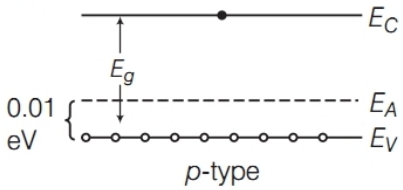
(ii) In energy band diagram of *n*-type semiconductor, the donor energy level E_D is slightly below the bottom of E_C conduction band and thus, the electron can move to conduction band, even with small supply of energy.



(1)

Characteristics features of *p*-type semiconductor

(i) In *p*-type semiconductor, the semiconductor is doped with trivalent impurity. In this semiconductor, the holes are the majority carriers and electrons are the minority carriers i.e. $n_h >> n_e$.



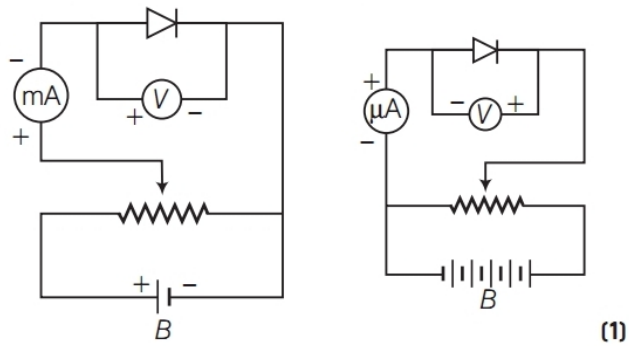
(ii) In energy band diagram of *p*-type, the acceptor energy level is slightly above the top of valence band E_V. Thus, even with small supply of energy electron from valence band can jump to level, E_A and ionise the acceptor, negatively. **(1)**

21. Differences between forward and reverse biasing are given below

Forward bias	Reverse bias
Positive terminal of battery is connected to *p*-type and negative terminal to *n*-type semiconductor.	Positive terminal of battery is connected to *n*-type and negative terminal to *p*-type semiconductor.
Depletion layer is very thin.	Depletion layer is thick.
p-n junction offers very low resistance.	*p-n* junction offers very high resistance.
An ideal diode have zero resistance.	An ideal diode have infinite resistance.

(1/2 × 4 = 2)

22. Circuit diagram of forward biased and reverse biased *p-n* junction diode is shown below



(1)

The width of depletion layer

(i) decreases in forward bias.

(ii) increases in reverse bias. **(1/2 × 2 =1)**

23. The four valence electrons of carbon are present in second orbit while that of silicon in third orbit. So, energy required to extricate an electron from silicon is much smaller than carbon.
Therefore, the number of free electrons for conduction in silicon is significant on contrary to the carbon. This makes silicon's conductivity much higher than carbon. This is the main distinguishable property. **(2)**

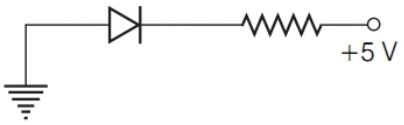
24. Refer to Sol. 13 on pages 409 and 410.

25. Refer to text on page 404.
(Formation of depletion region in *p-n* junction)
On applying forward bias, the width of the depletion region decreases.

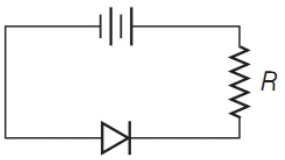
26. Refer to Sol. 13 on page 409. **(3)**

27. Refer to Sol. 13 on page 409. **(3)**

28. (i) The given diagram shown below.



The circuit above can be redrawn as follows



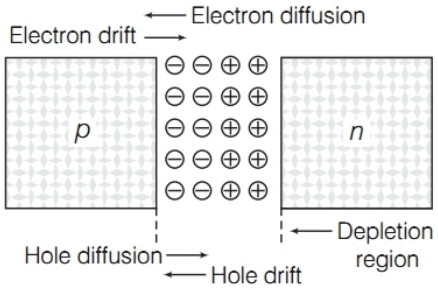
As, the p-section is connected to negative terminal of the battery, the diode shown is reverse biased. **(1)**

(ii) Refer to Sol. 13 on page 409.

29. Two processes that take place during the formation of p-n junction are diffusion and drift of charge carriers.

In a n-type semiconductor, the concentration of electrons is more than that of holes. Similarly, in a p-type semiconductor, the concentration of holes is more than that of electrons. Formation of depletion region during formation of p-n junction and due to the concentration gradient across p and n-sides, holes diffuse from p-side to n-side ($p \rightarrow n$) and electrons diffuse from n-side to p-side ($n \rightarrow p$). The diffused charge carriers combine with their counterparts in the immediate vicinity of the junction and neutralise each other. **(1)**

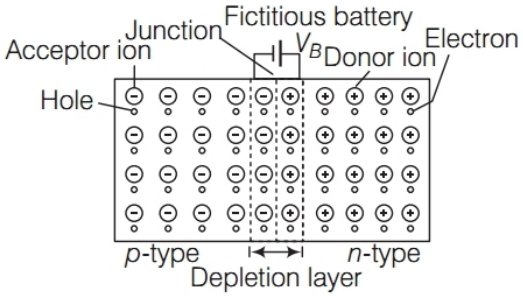
Thus, near the junction, positive charge is built on n-side and negative charge on p-side.



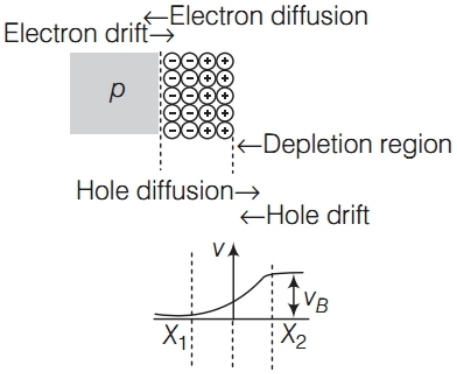
This sets up potential difference across the junction and an internal electric field E_i directed from n-side to p-side. The equilibrium is established when the field E_i becomes strong enough to stop further diffusion of the majority charge carriers (however, it helps the minority charge carriers to drift across the junction). **(1)**

The region on either side of the junction which becomes depleted (free) from the mobile charge carriers is called **depletion region** or depletion layer**.** The potential difference developed across the depletion region is called the **potential barrier**. **(1)**

30. (i) The small region in the vicinity of the junction which is depleted of free charge carriers and has only immobile ions is called **depletion region**.



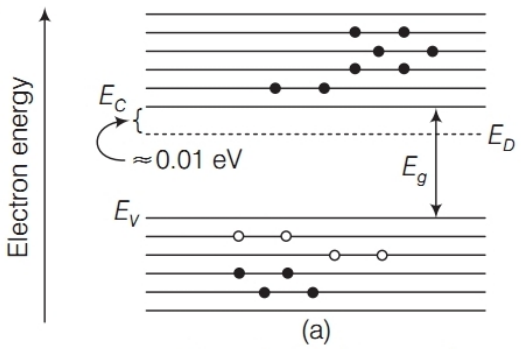
(1)



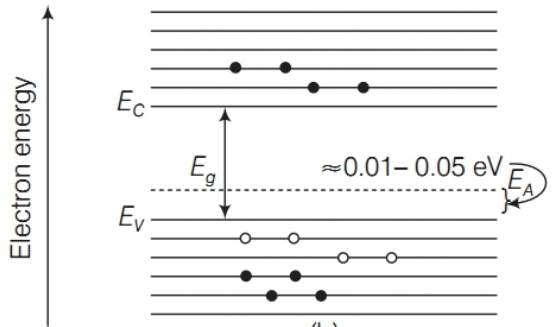
The accumulation of negative charges in the p-region and positive charge in the n-region sets up a potential difference across the junction. This acts as a barrier and is called barrier potential V_B.

(ii) Refer to Sol. 16 on page 410.

31. (i)



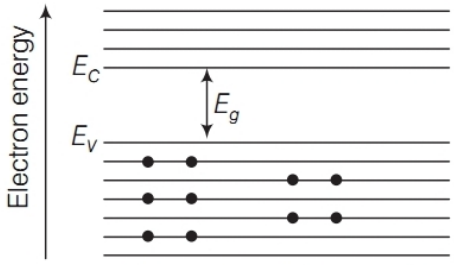
(a)
Energy band diagram of n-type semiconductor at $T>0$ K



(b)
Energy band diagram of
p-type semiconductor
at $T>0$ K

In *n*-type extrinsic semiconductors, the number of free electrons in conduction band is much more than the number of holes in valence band. The donor energy level lies just below the conduction band. In *p*-type extrinsic semiconductor, the number of holes in valence band is much more than the number of free electrons in conduction band. The acceptor energy level lies just above the valence band. **(1½)**

(ii)



Energy band diagram of
semiconductor at $T=0$ K

At absolute zero temperature (0 K), conduction band of semiconductor is completely empty, i.e., $\sigma=0$.

Hence, the semiconductor behaves as an insulator. At room temperature, some valence electrons acquire enough thermal energy and jump to the conduction band where they are free to conduct electricity. Thus, the semiconductor acquires a small conductivity at room temperature. **(1½)**

32. The required energy band diagrams are given in Sol. 31(i) on pages 412 and 413. **(2)**

The donor energy level E_D is just below the bottom of the conduction band. At room temperature, this small energy gap is easily converted by the thermally excited electrons. The conduction band has more electrons as they have been contributed both by thermal excitation and donor impurities. Whereas the acceptor energy level E_A lies slightly above the top of the valence band.

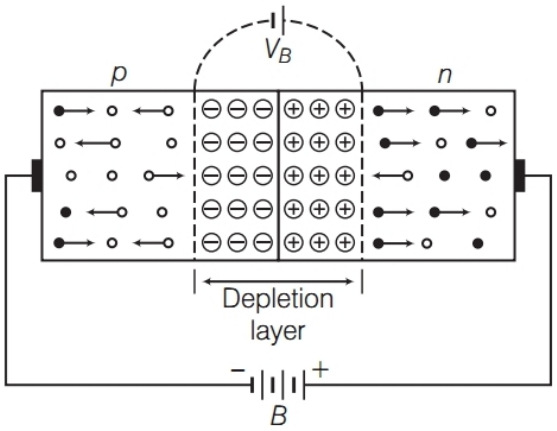
At room temperature, many electrons of the valence band get excited to these acceptor energy levels, leaving behind equal number of holes in the valence band. These holes can conduct current. Thus, the valence band has more holes than the electrons in the conduction band. **(1)**

33. Refer to text on page 402. **(3)**
(Differences between conductor, insulator and semiconductor on the basis of energy bands).

34. Refer to Sol. 13 on page 409. **(1)**

35. Refer to Sol. 13 on page 409. **(3)**

36.



During the formation of *p*-*n* junction, diffusion of charge takes place. As, soon as *p*-type semiconductor is joined with *n*-type semiconductor, diffusion of free charges across the junction starts. **(1)**

For explanation of formation of *p*-*n* junction
Refer to text on page 404 (*p*-*n* junction) **(1)**

Potential barrier The accumulation of '–ve' charges in the *p*-region and +ve charges in the *n*-region sets up a potential difference across the junction (*p*-*n*) is called potential barrier (V_B) which opposes the further diffusion of electrons and holes **(1)**

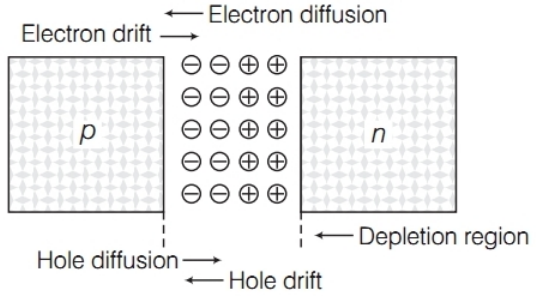
37. (i) Refer to Sol. 29 on page 412. **(2½)**

(ii) Refer to text on page 404.
(Forward Biased Characteristic) **(2½)**

38. (i) ***p*-*n* Junction** A *p*-*n* junction is an arrangement made by a close contact of *n*-type semiconductor and *p*-type semiconductor. There are various methods of forming *p*-*n* junction diode. **(1)**

Formation of Depletion Region in *p*-*n* Junction In an *n*-type semiconductor, the

concentration of electrons is more than concentration of holes. Similarly, in a *p*-type semiconductor, the concentration of holes is more than that of concentration of electrons. During formation of *p*-*n* junction and due to the concentration gradient across *p* and *n*-sides, holes diffuse from *p*-side to *n*-side ($p \rightarrow n$) and electrons diffuse from *n*-side to *p*-side ($n \rightarrow p$).

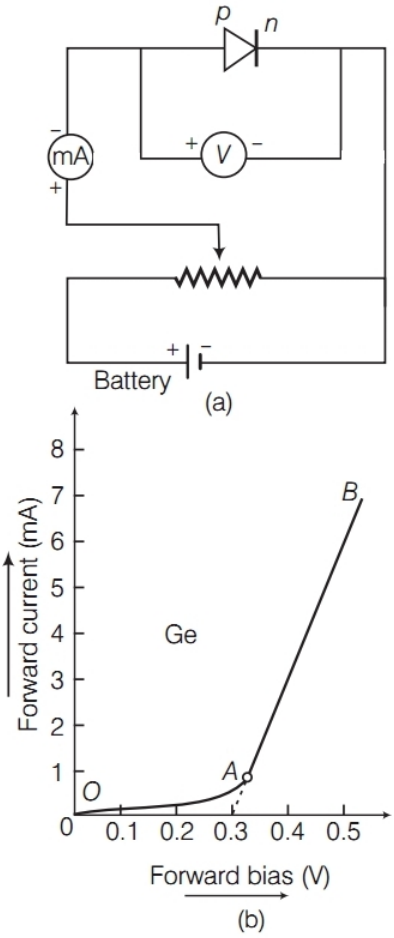


The diffused charge carriers combine with their counterparts in the immediate vicinity of the junction and neutralise each other. **(1)**

Thus, near the junction, positive charge is built on *n*-side and negative charge on *p*-side. This sets up potential difference across the junction and an internal electric field E_i directed from *n*-side to *p*-side. The equilibrium is established when the field E_i becomes strong enough to stop further diffusion of the majority charge carriers (however, it helps the minority charge carriers to diffuse across the junction). The region on either side of the junction which becomes depleted (free) from the mobile charge carriers is called depletion region or **depletion layer.** The width of depletion region is of the order of 10^{-6} m. The potential difference developed across the depletion region is called the **potential barrier**. Potential barrier depends on dopant concentration in the semiconductor and temperature of the junction. **(1)**

(ii) (a) **Forward Biased Characteristics**

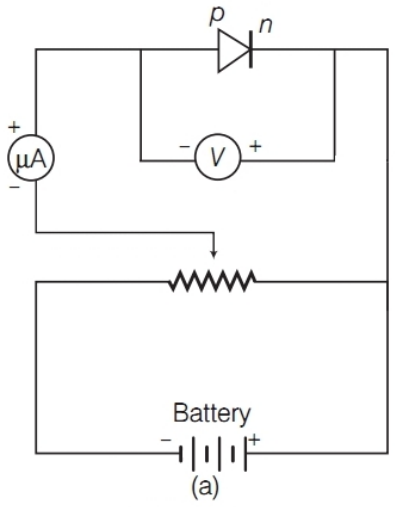
The circuit diagram for studying forward biased characteristics is shown in the figure. Starting from a low value, forward bias voltage is increased step by step (measured by voltmeter) and forward current is noted (by ammeter). A graph is plotted between voltage and current. The curve so obtained is the forward biased characteristic of the diode.

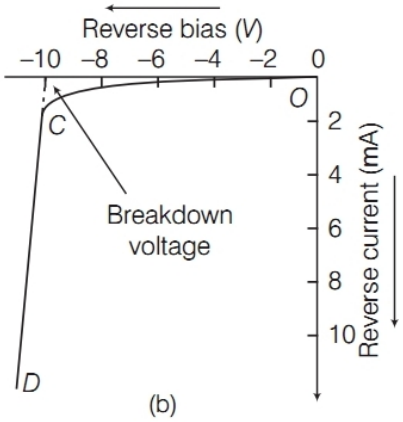


At the beginning, when applied voltage is low, the current through the diode is almost zero. It is because of the potential barrier, which opposes the applied voltage. Till the applied voltage exceeds the potential barrier, the current increases very slowly with increase in applied voltage (*OA* portion of the graph*)*.With further increase in applied voltage, the current increases very rapidly (*AB* portion of the graph), in this situation, the diode behaves like a conductor. The forward voltage beyond which the current through the junction starts increasing rapidly with voltage is called **knee voltage**. If line *AB* is extended back, it cuts the voltage axis at potential barrier voltage. **(1)**

(b) **Reverse Biased Characteristics**

The circuit diagram for studying reverse biased characteristics is shown in the figure.





In reverse biased, the applied voltage supports the flow of minority charge carriers across the junction. So, a very small current flows across the junction due to minority charge carriers.

Motion of minority charge carriers is also supported by internal potential barrier, so all the minority carriers cross over the junction.

Therefore, the small reverse current remains almost constant over a sufficiently long range of reverse bias, increasing very little with increasing voltage (*OC* portion of the graph). This reverse current is voltage independent upto certain voltage known as **breakdown voltage** and this voltage independent current is called **reverse saturation current**.

Use of *p-n* Junction Characteristics in Rectification

From forward and reverse characteristics, it is clear that current flows through the junction diode only in forward bias not in reverse bias i.e. current flows only in one direction. **(1)**

39. (i) Refer to Sol. 38 (i) on pages 413 and 414. **(3)**

(ii) Refer to Sol. 13 on page 409. **(2)**

40. (i) Refer to Sol. 38(i) on page 413 and 414. **(1)**

(ii) Refer to Sol. 13 on page 409. **(1)**

(iii) A full-wave bridge rectifier using four diodes (full-wave bridge rectifier) gives a continuous, unidirectional but pulsating output voltage or current. **(1)**

The rectified output is passed through a filter circuit which removes the ripple and an almost steady DC voltage (or current) is obtained. **(2)**